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Chapter 7

Readout Electronics

7.1 Overview

The goal of the GLUEX readout electronics system is to digitize and read out the detector signals for level 1 trigger rates of up to 200 *kHz* without incurring deadtime. A pipelined approach is required. The digitized information will be stored for several μs while the level 1 trigger is formed. Multiple events must be buffered within the digitizer modules and read while the front ends continue to acquire new events.

Two basic types of readout electronics will be used in GLUEX, FADCs and TDCs. Detectors which measure energy will be continuously sampled with flash ADCs while detectors which require precise time measurements will use a multi-hit TDC. No currently available commercial solutions exist. These boards will be designed by our collaboration. Prototypes have been constructed, and are being tested.

The number of channels in the GLUEX detector is not large enough to justify the financially risky development of custom integrated circuits. Programmable logic devices are fast enough and available at reasonable cost. Programmable logic also allows for optimization of the data path without redesigning a printed circuit. ICs developed for other experiments will also be used.

Electronics technology is constantly evolving, and the optimum solution for the GLUEX detector depends on when funding becomes available and the construction schedule. Presented here is a preliminary design which could be implemented with currently available components.

7.2 FADCs for Calorimetry

The calorimeters will be read out with 8-bit, 250 *MHz* linear FADCs. The 250 *MHz* sampling clock will be derived from the 1499 *MHz* accelerator clock. This sampling rate and bit depth is well matched to the FEU84-3 PMTs used in the Forward Calorimeter, and to the hybrid PMTs used in the Barrel Calorimeter. Additional FADC channels will be used for gain matching and monitoring of the Photon Tagger, Start Counter, Čerenkov Detector, and Time of Flight PMTs.

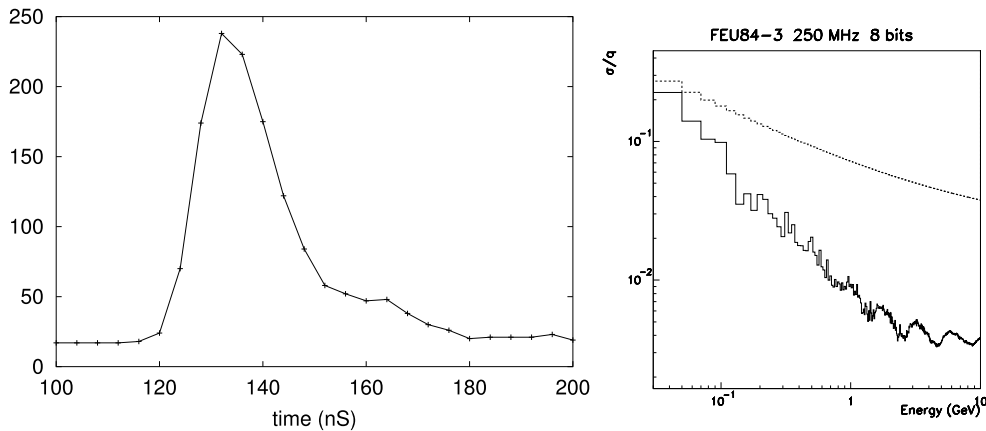


Figure 7.1: **Left:** Digitized FEU84-3 pulse. **Right:**Resolution as a function of energy for simulated FEU84-3 PMT sampled at 8 bits, 250 MHz. LGD resolution is shown by dotted line. FADC samples are summed to determine energy.

Figure 7.1(left) shows an FEU84-3 PMT pulse digitized by the prototype FADC described in section 7.2.1. Note that the sum of the samples from 120 to 180 *ns* is 1429; for this PMT the 8-bit FADC is equivalent to a 10 or 11-bit conventional charge-integrating ADC. To address resolution concerns, simulations were performed to show that the proposed FADC provides an adequate measurement. Pulses measured with a digital oscilloscope were fitted to determine their functional form. The response of the FADC was simulated using this functional form and the time integral of the function was compared to the summed output of the simulated FADC for many pulses. Since the relationship between deposited energy and pulse height in this type of calorimeter is known, direct comparison of the resolution due to the FADC and the resolution of the calorimeter is possible. Figure 7.1(right) shows the result of this comparison. Clearly, above 0.15 *GeV* the resolution of the FADC is small compared the the intrinsic resolution of the calorimeter.

The FADCs will also give a measurement of the time a photon arrived at the calorimeter. Previous work [1, 2] indicates that a time resolution better than the FADC sampling interval can be achieved by fitting the FADC waveform. To study how well this time could be determined a “library” of pulses from phototubes of the type to be used was created using a digital oscilloscope with a 2.5 *GHz* sampling frequency. The leading edge of these sampled pulses were fitted to a 9th order polynomial to determine the location of various “features” of the pulses. The features considered were the time the pulse achieved 10, 25, 50, 75, 90 and 100% of its maximum value. These features carry the arrival time information of the pulses and were used as reference times.

To determine how well the FADC could determine the pulse arrival time, the samples from the digital oscilloscope (2.5 *GHz*) were averaged over 10 samples (to 250 *MHz*) and quantized to 8 bits. These transformed samples are what would be expected from the FADC system proposed here. Using only the bin containing the pulse maximum and the two samples preceding it and a simple algorithm, it was found that the 50% crossing time could be determined with a resolution of 160 *ps* compared to the time determined by the detailed fitting described above. This resolution is sufficient to determine if a pulse is in time with an event (rejecting background) or to determine the time of the event sufficiently well to select the beam “bucket” that initiated the event.

7.2.1 Prototype

A single channel prototype of the calorimeter FADC has been designed and built at Indiana University. A block diagram is shown in Fig. 7.2 and a photo in Fig. 7.3.

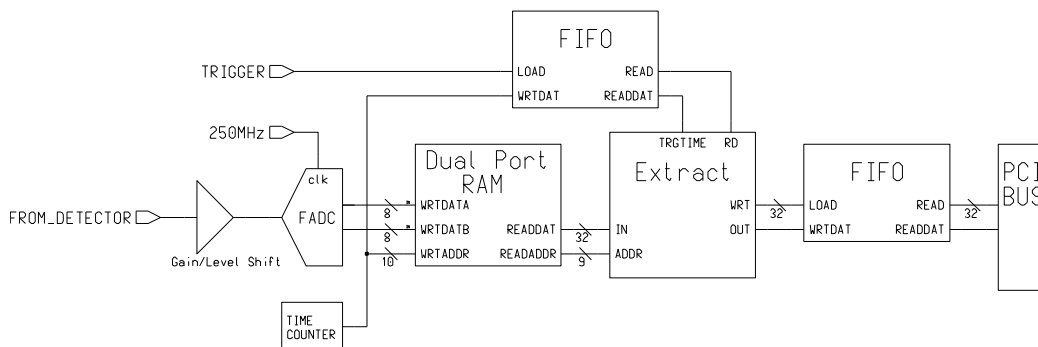


Figure 7.2: Block diagram of prototype FADC board.

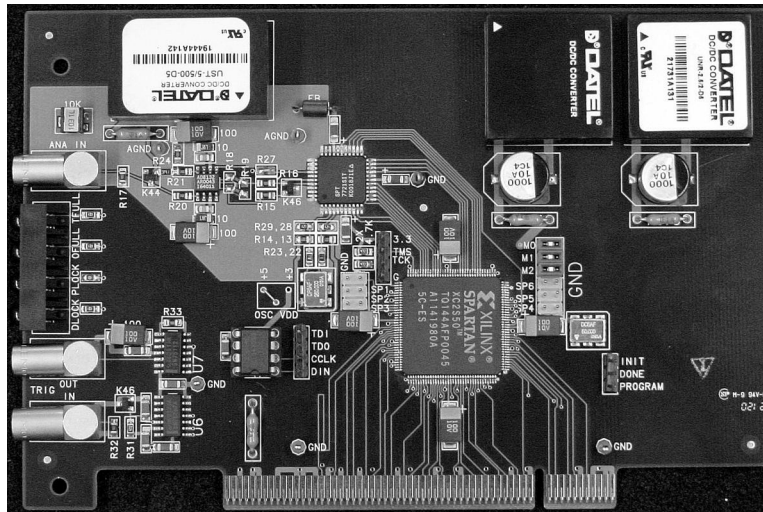


Figure 7.3: Photograph of prototype FADC board.

A differential amplifier inverts the negative PMT signal and shifts the voltage levels to match the input range of the digitizer integrated circuit. The digitization is performed by an SPT7721 integrated circuit manufactured by Signal Processing Technologies [3]. This IC costs about US\$25 each in small quantities. An 8-bit value is produced internally every 4 ns ; two samples are output every 8 ns (125 MHz).

All digital functions are performed in a Xilinx [4] XC2S50 programmable gate array. This IC costs about US\$15 each in small quantities. A dual port RAM configured as a circular buffer stores the data for 8 microseconds. Upon receipt of a trigger signal the data from the time window of interest is copied to an output FIFO which can buffer the data from multiple events. This FIFO is interfaced to a 32 bit, 33 MHz PCI bus. More information on this prototype is available [5].

7.2.2 Additional requirements for final version

The final version of the calorimeter FADC board will include pipelined adders operating at the 125 MHz digitizer output clock which continuously sum the digitized information from all channels on a board. Additional pipelined adders will sum the information from all boards in a crate, and then sum the information from all the crates associated with a detector. The sum of all channels will be passed through a shift register giving a time history. Successive samples within a programmable time window will be summed, analogous to the gate

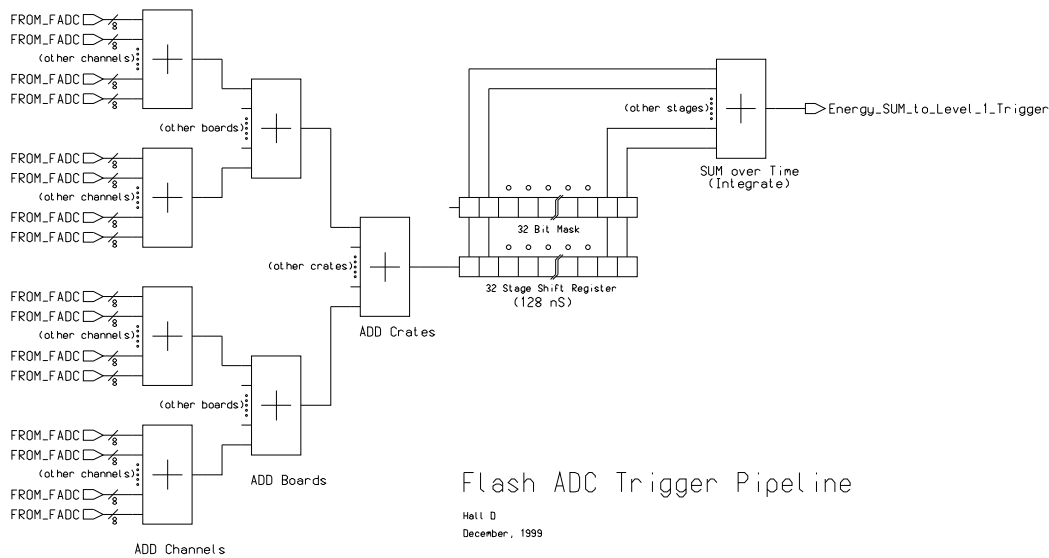


Figure 7.4: Block diagram of energy sum.

width in a conventional charge sensitive ADC. This energy sum will be used in the level 1 trigger. A block diagram is shown in Fig. 7.4.

Assuming a 100 ns time window, each FADC channel will produce 25 bytes of data per level 1 trigger. In the final version of the FADC we will want to suppress the readout of channels with no data. The FADC data will be processed in real time to provide an energy and time measurement. We believe that the raw FADC data can be reduced to about 10 bytes per channel. This zero suppression and pulse shape processing may be done at the channel level in the gate array, at the board level, the crate level, the detector system level, or in some combination of these levels.

7.3 FADCs for Tracking

The Central Tracking Drift Chamber anodes will be read out with 8-bit, 250 MHz nonlinear FADCs. The digitizer will be preceded by a logarithmic amplifier which will compress a 10-bit dynamic range down to 8 bits. This additional dynamic range is required for the dE/dx measurement.

The Forward Tracking Drift Chamber cathodes will produce positive polarity signals. These signals are relatively slow, and may be sampled by 125 or possibly 62.5 MHz FADCs.

The adders for the energy sum will not be needed on the tracking FADCs.

7.4 TDCs

The Photon Tagger, Start Counter, Vertex Tracker, Forward Drift Chamber anodes, Čerenkov Detector, Barrel Calorimeter, and Time of Flight Wall will be read out by multi-hit TDCs.

7.4.1 Prototype

Such a high resolution pipeline TDC module has been developed for use at Jefferson Lab, and is designed to meet the requirements of current experiments, as well as to serve as a prototype for future experiments, including Hall D. The design is implemented as a VME-64x module. This bus standard was chosen because it is already in use at Jefferson Lab, has good (and evolving) data transfer capabilities, and reasonable channel densities are possible. A block diagram is shown in Fig. 7.5 and a photo in Fig. 7.6.

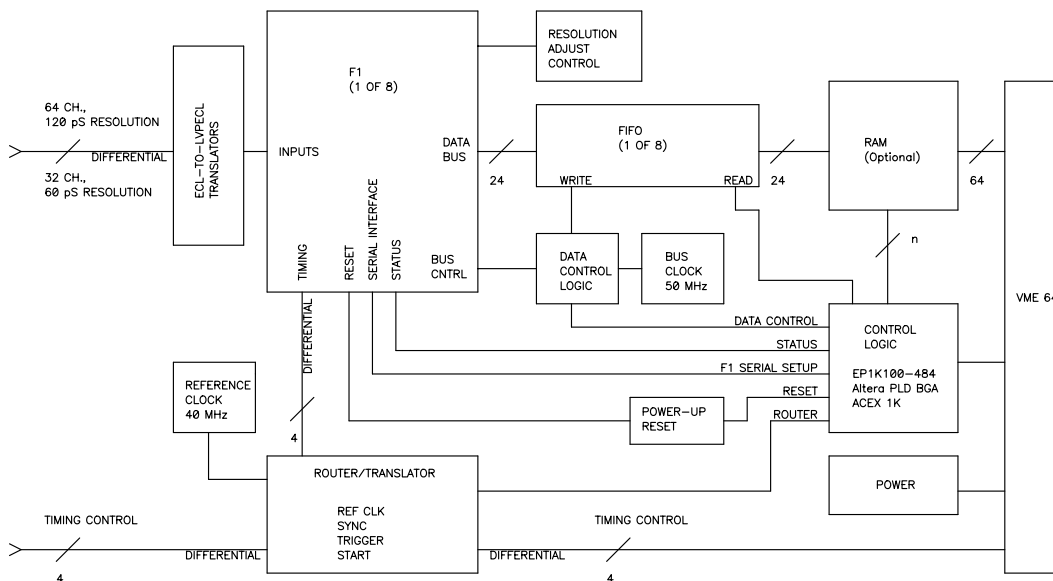


Figure 7.5: Block diagram of prototype TDC board.

unnamed

The module is built around the TDC-F1 integrated circuit from Acam-Messelectronic GmbH [6], originally designed for the COMPASS experiment at CERN [7]. This chip costs about US\$130 each in small quantities. It includes many features that will be useful in experiments at Jefferson Lab. This chip utilizes purely digital delay techniques to measure time. In normal mode the TDC-F1 chip provides 8 input channels with up to 120 ps resolution (LSB).

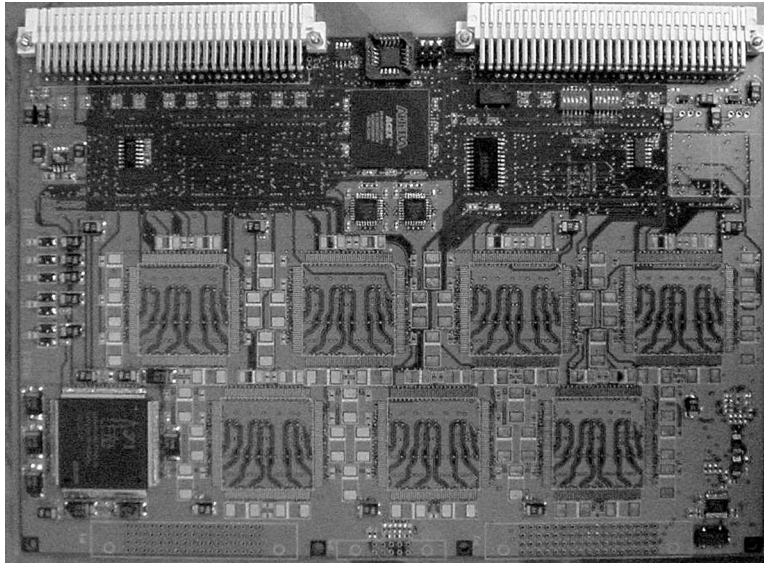


Figure 7.6: Photograph of prototype TDC board.

In high resolution mode channels are combined in pairs to yield up to 60 ps resolution for 4 input channels. The dynamic range for measurement is 16 bits. The resolution of the chip is tunable about its nominal value. A PLL circuit adjusts the core voltage of the chip to compensate for temperature and supply voltage variation, assuring stability of the resolution value. On-chip buffering for input channels, triggers, and output data allows for multihit operation with nearly zero deadtime. The chip also has a complex trigger matching unit that can filter out hits unrelated to the input trigger. When enabled, only hits that are within a programmed timing window relative to the trigger time are kept.

The 8 TDC-F1 chips on our module provide 64 channels in normal mode, or 32 channels in high resolution mode. A 128K word deep FIFO is attached to each TDC-F1 chip to buffer its output data. The module can be set up to interrupt the crate controller after a programmable number of triggers have been received. During read out the module will provide a block of data associated with a programmed number of triggers, and then terminate the transaction. To enhance system performance a set of TDC modules may be read out as a single logical read using a multiblock read protocol. This involves passing a token between modules along a VMEbus daisy-chain line. In this setup, only the first module in the chain will generate the interrupt, and only the last module in the chain will terminate the transaction.

The TDC module is fabricated as a single 12-layer printed circuit board. Six of these layers carry signals on 5 mil wide traces. Internal layers are

organized in a stripline configuration and have a characteristic impedance of 50 ohms. High-speed ECL components are used for the front end. Logic in a single FPGA chip (484-pin BGA) controls the entire module. The high density of the design demands that surface mount components be installed on the front and back sides of the board.

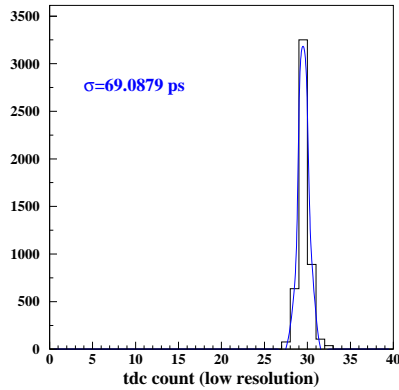


Figure 7.7: TDC performance in low resolution.

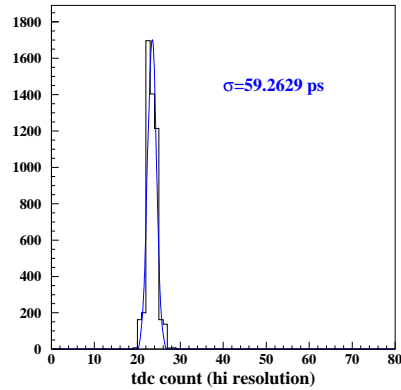


Figure 7.8: TDC performance in high resolution.

7.4.2 Initial test results

The layout and power sections of the bare boards were tested and verified, and then the programmable logic IC using a ball grid array package was installed by industry. Programmable logic was loaded and tested successfully. We then proceeded with initial tests of the the F1 chip itself. The prototype was outfitted with a single F1 chip, corresponding to eight channels of low (normal) resolution, or four channels of high resolution. All channels were found to be operational and tested for performance. Timing signals were generated with a Highland V851 digital delay generator with a measured jitter of approximately 30 ps¹. The time calibration at low resolution was found to be 115.1 ps/count (120 ps/count nominal) and 57.5 ps/count in high resolution (60 ps/count nominal). The time resolution of two typical channels are shown in Figs. 7.7 and 7.8 indicating $\sigma = 69$ ps in low resolution and $\sigma = 59$ ps in high resolution. Subtracting the contribution from the time generator we obtain 62 ps and 51

¹The V851 specifications for jitter is 25 ps.

ps for the prototype performance in low and high resolution respectively. This is to be compared with the quoted rms resolution of the F1 chip of 40 ps .

7.4.3 Additional requirements for final version

A common clock will be distributed to all TDC modules so that every channel has the same time calibration. It may be desirable to derive this clock from the accelerator clock, in which case the LSB resolution would be 125 ps for the standard version and 62.5 ps for the high resolution version. The Start Counter, Barrel Calorimeter, and Time of Flight detectors will require pipelined adders to implement a track count for use in the level 1 trigger. These adders may be part of the high resolution version of the TDC board, or on a separate board.

7.5 Discriminators and Amplifiers

Detectors which provide precise timing (Photon Tagger, Start Counter, Barrel Calorimeter, and Time of Flight counters) will require “constant fraction” discriminators. Ideally these discriminators would be built-in as part of the PMT bases. The Čerenkov detector, Forward Drift Chamber anodes and Vertex Tracker fibers can probably use conventional discriminators. For optimum performance the chamber discriminators should be mounted directly on the chamber itself, inside the solenoid. It may be possible to use the “ASD” ICs developed for the Atlas [8] detector. The Central Drift Chamber anodes and Forward Drift Chamber cathodes will need an amplifier to drive the FADC inputs. These amplifiers should be located on the chambers if possible.

7.6 Scalers and Latches

For compatibility with the FADCs and TDCs, any scalers and latches must also be pipelined. Upon receipt of a level 1 trigger, the scaler values must be transferred to an output buffer while the scalers continue to count. Latch patterns must also be transferred to an output buffer and later read out without interfering with incoming triggers. Unless a commercial solution becomes available, these boards will be designed by our collaboration.

7.7 High Voltage

The Forward Calorimeter PMTs will be powered by Cockcroft-Walton voltage multipliers [9] which will be built at Indiana University. This type of base provides for the very low power consumption necessary for such a tightly packed array and is controlled over a serial communication link. The Barrel Calorimeter, Čerenkov, Time of Flight, and Start Counter PMTs may be powered by similar circuitry. These PMT bases need built-in discriminators if possible, as noted in section 7.5. The Tracking Chambers will probably be powered by commercial HV power supplies with sensitive current monitoring.

7.8 Packaging

The FADC circuit requires about 50 cm^2 of board space and adjacent channels will need to be about 2 - 3 cm apart. This implies a density of about 8 channels on a 6U board or possibly 16 channels on a 9U board.

In the low resolution (120 ps) version of the TDC 64 channels fit on a 6U board. This version of the TDC is used for the Forward Drift Chamber anodes, Vertex Tracker fibers, and the Čerenkov detector .

The Photon Tagger, Start Counter, Barrel Calorimeter, and Time of Flight counters require the high resolution (60 ps) version of the TDC. This version of the TDC has 32 channels per 6U board.

Assuming a maximum of 20 6U boards in a crate, and 4 crates in a rack, table 7.1 summarizes the space required.

The readout electronics will be located as close to the detector as possible to minimize signal cable runs. Note that the Tagger electronics will be located in a separate building 80 m upstream of the main detector. The Time of Flight and Forward Calorimeter electronics will be downstream of these detectors. Cabling from detectors inside the solenoid will exit at the upstream and downstream ends of the magnet and connect to nearby electronics. Fiber optic cables will transport the data from the readout processors to the level 3 trigger processor farm in the GLUEX counting house.

7.9 Readout Bus

FASTBUS crates are no longer being manufactured, and FASTBUS is not being considered for GLUEX. CAMAC crates are fairly slow and have limited board space and power available. Some legacy devices like discriminators,

Board type	Detector	Channels	Modules	Crates	Racks
Linear FADC	Photon Tagger Counters	250	32	2	1/2
Linear FADC	Start Counters	10	2		
Linear FADC	Barrel Calorimeter	576	72	4	1
Linear FADC	Čerenkov Detector	38	5	1/4	
Linear FADC	Time of Flight Counters	320	40	2	1/2
Linear FADC	Forward Calorimeter	2200	275	16	4
Linear FADC	Upstream Veto	21	3	1/4	
Logarithmic FADC	Central Drift Anodes	3360	420	21	6
Positive FADC	Forward Drift Cathodes	5760	720	36	9
120 <i>ps</i> TDC	Vertex Tracker Fibers	2000	32	2	1/2
120 <i>ps</i> TDC	Forward Drift Anodes	2880	45	3	3/4
120 <i>ps</i> TDC	Čerenkov Detector	38	1		
60 <i>ps</i> TDC	Photon Tagger Counters	250	8	1/2	
60 <i>ps</i> TDC	Polarimeter	2048	64	4	1
60 <i>ps</i> TDC	Start Counters	10	1		
60 <i>ps</i> TDC	Barrel Calorimeter	576	18	1	1/4
60 <i>ps</i> TDC	Time of Flight Counters	320	10	1/2	
60 <i>ps</i> TDC	Upstream Photon Veto	21	1		
Totals				94	24

Table 7.1: A summary of the electronics channels and space required.

trigger logic or HV supplies which are not part of the data readout may be packaged in CAMAC, but not the bulk of the readout electronics.

VME is popular at Jefferson Lab and the TDC prototype is constructed on a VME64x card. Compact PCI is used extensively in the telecommunications industry and can be driven directly by typical FPGA ICs without the need for bus interface ICs. Predefined PCI interface “cores” are available, minimizing design time. One disadvantage of cPCI is that bridges are required for a system with more than 8 slots, although commercial bridges which consume no slots are available.

VXI and PXI are “instrumentation” extensions to VME and cPCI. Shielding, triggering, clock distribution, and additional power are added to the basic bus standard.

The FADCs require a low skew fanout of the 250 *MHz* clock, a synchronization signal, and the level 1 trigger. The need to form a digital global energy sum for the level 1 trigger will probably drive the choice of packaging for the

calorimeter FADCs. Some sort of custom backplane will be required to support the trees of adders which form the energy sum and track counts.

The telecommunications industry is moving towards “Switched Serial Fabrics.” This adds a high speed serial connector to the backplane which can support Ethernet and other high speed serial technologies. For VME the applicable standard is VXS (VITA 41) and for cPCI the standard is cPSB (PICMG 2.16). For a 16 channel FADC module producing 25 bytes per channel per level 1 trigger; a level 1 trigger rate of 200 *kHz*; and a 2% occupancy the data readout bandwidth required for a module is 16 Megabits per second, well within the capability of a 100baseT Ethernet connection.

7.10 Construction

Indiana University has experience building large electronic systems for experiments at Fermilab, Brookhaven, and Jefferson Lab. The GLUEX experiment is larger and more complex than past experiments and will require the development of new techniques. High reliability is crucial to the success of the GLUEX experiment. We plan to begin long term tests of GLUEX electronics as soon as they are produced giving early identification of problems and failure modes.

Producing electronics assemblies in house has several advantages over having a commercial firm doing the assembly. To achieve the lowest cost, a commercial service would assemble a large batch all at once. This risks learning about problems after it’s too late to change anything. Assembling smaller batches in house allows immediate feedback to the assembly process.

The lifetime of the GLUEX experiment will be long enough that we must plan for maintenance and repair of the custom electronics. Sufficient spare parts must be purchased at construction time to avoid the risk of a component manufacturer discontinuing some crucial part. Spreading the purchase of components over too long a time also risks some components becoming unavailable.

We plan to make use of robotic electronic assembly technology both for initial construction and for replacing defective components. Such a device [10] can selectively install and remove components without disturbing nearby devices. This would facilitate building a board in stages and testing partial assemblies, a technique especially useful in producing the Cockcroft-Walton PMT bases.

7.11 Manpower

Core manpower exists at Jefferson Lab and Indiana University and is sufficient for preliminary R&D studies. However, actually building, commissioning and running the GLUEX electronics will require additional manpower both at Jefferson Lab and at collaborating institutions.

There are several areas where additional collaborators with electronics expertise would be welcome. The VLPCs proposed for the Vertex Tracker scintillating fiber readout are an unusual technology, and no experience exists within the collaboration. Constant fraction discriminators for the detectors which produce precise times need to be developed and integrated into the PMT bases. The discriminators and preamps for the Tracking drift chambers will need to be adapted from other experiments. Algorithms for reducing the FADC data volume need further development.

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